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DESIGN AND PERFORMANCE EVALUATION OF A HIGH-VOLTAGE DC GENERATOR USING A COCKCROFT-WALTON MULTIPLIER

DESAIN DAN EVALUASI KINERJA GENERATOR DC TEGANGAN TINGGI MENGGUNAKAN MULTIPLIER COCKCROFT-WALTON

Turahyo[1*], Noviarianto[2]
[1*] Sekolah Tinggi Teknologi Bontang, Email: turahyoahyo@gmail.com
[2] Sekolah Tinggi Teknologi Bontang, Email: novi@polimarin.ac.id

*email koresponden: turahyoahyo@gmail.com

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Abstract

This paper presents the design and performance evaluation of a high-voltage direct current (DC) generator based on the Cockcroft–Walton (CW) voltage multiplier for laboratory-scale applications in electrical engineering. Conventional high-voltage generation methods often involve bulky transformers and complex circuitry, making them less suitable for compact and cost-effective laboratory use. To address these limitations, a modular CW-based system is proposed, integrating a high-frequency input source with an optimized diode-capacitor ladder network. The proposed system is designed to achieve high DC voltage output in the kilovolt range while maintaining acceptable levels of ripple and efficiency. Experimental results show that the system can achieve up to 86% of the theoretical output voltage under no-load conditions, with an efficiency of around 70.8%. Furthermore, the ripple voltage of the generated output voltage is very small, demonstrating stable performance suitable for laboratory applications. The proposed design offers a compact, cost-effective, and reliable solution for high-voltage DC generation, making it highly suitable for educational and low-power applications.

Keywords : Voltage Multiplier, Cockcroft–Walton Multiplier, DC High-Voltage, Ripple Voltage, Electrical Engineering.

Abstrak

Makalah ini menyajikan desain dan evaluasi kinerja generator arus searah (DC) tegangan tinggi berbasis pengali tegangan Cockcroft–Walton (CW) untuk aplikasi skala laboratorium di bidang teknik elektro. Metode pembangkitan tegangan tinggi konvensional seringkali melibatkan transformator besar dan rangkaian yang kompleks, sehingga kurang cocok untuk penggunaan laboratorium yang ringkas dan hemat biaya. Untuk mengatasi keterbatasan ini, sistem berbasis CW modular diusulkan, yang mengintegrasikan sumber input frekuensi tinggi dengan jaringan tangga dioda-kapasitor yang dioptimalkan. Sistem yang diusulkan dirancang untuk mencapai keluaran tegangan DC tinggi dalam kisaran kilovolt sambil mempertahankan tingkat riak dan efisiensi yang dapat diterima. Parameter desain utama, termasuk jumlah tahapan, nilai kapasitansi, dan frekuensi switching, dipilih dan dianalisis dengan cermat. Hasil eksperimen menunjukkan bahwa sistem dapat mencapai hingga 86% dari tegangan keluaran teoritis dalam kondisi tanpa beban, dengan efisiensi berkisar 70.8%. Lebih lanjut, tegangan riak dari tegangan keluaran yang dihasilkan sangat kecil. Hal ini menunjukkan kinerja stabil yang cocok untuk aplikasi laboratorium. Desain yang diusulkan menawarkan solusi yang

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ringkas, hemat biaya, dan andal untuk pembangkitan DC tegangan tinggi, sehingga sangat cocok untuk aplikasi pendidikan dan aplikasi berdaya rendah.

Kata Kunci : Pengganda Tegangan, *Cockcroft-Walton*, Tegangan Tinggi DC, Tegangan Riak, Teknik Elektro.

1. INTRODUCTION

The demand for high-voltage DC (High Voltage Direct Current (HVDC) generation systems continues to grow along with the development of applications in modern electrical engineering, such as high-voltage insulation testing, industrial electrostatic systems, plasma technology, medical equipment, and renewable energy systems based on advanced power conversion. In this context, high-voltage generation systems are required not only to produce high voltage levels but also to possess superior performance characteristics, including high efficiency, low ripple, stability against load variations, and ease of implementation (Erickson & Maksimović, 2020; Rashid, 2021). However, conventional approaches based on low-frequency transformers or high-voltage isolation converters often face limitations such as large size, design complexity, and significant power losses (Mohan et al., 2020; Hart, 2022). This drives the need for simpler alternative approaches that still meet the performance demands of modern systems.

One widely used solution is the Cockcroft–Walton (CW) voltage multiplier, which offers a voltage boosting method based on a cascaded diode-capacitor network. This topology is known for its advantages in terms of simple structure, low implementation costs, and the ability to generate high voltages without the need for complex high-voltage transformers. A study by Kenfack et al. (2022) showed that CW multipliers are capable of generating high DC voltages with competitive efficiency in low- to medium-power applications. Furthermore, a study by Zarepour et al. (2021) confirmed that the integration of CW multipliers in an AC-DC rectifier system can produce a high voltage gain ratio with a minimal number of active components, thereby increasing system reliability.

Despite its structural advantages, the practical performance of CW multipliers is still limited by a number of fundamental issues, particularly those related to the system's dynamic characteristics. These include output voltage sag due to load effects, a significant increase in voltage ripple at a large number of stages, and reduced efficiency due to accumulated losses at each stage. Wang et al. (2025) emphasized that multistage charge pump design requires careful parameter optimization to maintain high efficiency, especially under dynamic load conditions. Murad et al. (2020) also showed that switching frequency and input source configuration significantly influence the overall performance of a CW multiplier. Thus, although CW multipliers are theoretically capable of producing very high voltages, their actual performance is highly dependent on design strategy and operational conditions.

Various approaches have been proposed to overcome these limitations. Mardiyah et al. (2024) developed a push-pull inverter-based system to improve input voltage stability and reduce output fluctuations. Meanwhile, Jaiwanglok et al. (2020) proposed a structural modification of the CW multiplier to increase voltage gain while reducing ripple. Another study by Altimania et al. (2020) showed that the use of multiplier cells in certain configurations can significantly improve the voltage conversion ratio. In fact, recent approaches have begun to integrate artificial intelligence-based techniques to more accurately model and predict voltage ripple, as demonstrated by Islam (2025). Furthermore, research by Akiyama et al. (2025) indicates that CW multipliers have great potential for in-situ high-voltage generation applications in next-generation power electronics systems.

However, based on a review of the existing literature, several research gaps remain unaddressed. First, most research focuses on improving CW multiplier performance at the industrial scale or for specific applications, while implementations optimized for educational laboratory environments are relatively limited. Second, there is no design approach that explicitly considers the trade-offs between the number of stages, system efficiency, and output voltage quality in the context of safe and economical practical applications.

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Furthermore, some previous studies tend to evaluate CW multiplier performance partially, for example, focusing only on output voltage or efficiency, without examining the interdependencies between these parameters. However, in real-world implementations, these parameters interact nonlinearly. For example, increasing the number of stages can increase output voltage, but at the same time, it can also increase ripple and decrease system efficiency. Therefore, a more holistic, experiment-based design approach is needed to fully understand the system's characteristics (Evans et al., 2017; Al-Mamoori et al., 2019).

Based on this background, this study proposes a high-voltage DC power generation system design based on a Cockcroft–Walton multiplier integrated with a high-frequency inverter as the input source. The approach used in this study focuses not only on circuit implementation but also includes an analysis of system performance based on variations in the number of stages.

THEORETICAL BACKGROUND

Principle of Cockcroft–Walton Voltage Multiplier

The Cockcroft–Walton (CW) voltage multiplier is a well-known circuit topology used to generate high DC voltages from a relatively low AC or pulsating DC input. It operates based on a ladder network consisting of capacitors and diodes arranged in a cascaded configuration. The fundamental working principle relies on sequential charging and discharging of capacitors during alternating half-cycles of the input signal, resulting in voltage stacking across multiple stages. In an ideal CW multiplier with nnn stages, the output voltage can be approximated as:

$$Vout = 2nVp \qquad (01)$$

where:
Vout = output DC voltage
n = number of stages
Vp = peak input voltage

This equation assumes ideal conditions, neglecting diode voltage drops, parasitic resistance, and load effects. In practice, the output voltage is always lower due to non-idealities in components and circuit behavior.

Voltage Drop and Ripple Analysis

In real-world applications, the performance of a CW multiplier is significantly influenced by voltage drop and ripple. These effects arise due to the finite capacitance values, load current, and switching frequency of the input source. The voltage drop (ΔV) in a CW multiplier under load can be expressed as:

$$\Delta V = \frac{I}{fC} \cdot \frac{n(n+1)}{2} \qquad (02)$$

where:
I = load current
f = input frequency
C = capacitance per stage
n = number of stages

This relationship indicates that voltage drop increases quadratically with the number of stages, which becomes a critical limitation when designing high-voltage systems. Similarly, the output voltage ripple (Vripple) can be approximated as:

$$Vripple = \frac{I}{fC} \cdot n \qquad (03)$$

Efficiency Considerations

The efficiency of the CW multiplier is affected by several factors, including diode losses, capacitor leakage, and switching losses. The overall efficiency (η\etaη) can be expressed as:

$$\eta = \frac{Pout}{Pin} \times 100\% \qquad (04)$$

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Losses in the system are mainly caused by several problems, including: forward voltage drop across diodes, equivalent series resistance (ESR) of capacitors and leakage currents in high-voltage components. As the number of stages increases, cumulative losses also increase, which can significantly reduce efficiency. Therefore, an optimal trade-off between output voltage level and efficiency must be carefully considered during the design process.

2. RESEARCH METHOD

The proposed high-voltage DC generator system is designed based on a modular architecture that integrates a low-voltage input source, a high-frequency switching stage, and a Cockcroft–Walton voltage multiplier network. System is intended to produce a stable high-voltage DC output suitable for laboratory-scale applications while maintaining simplicity, safety, and cost-effectiveness.

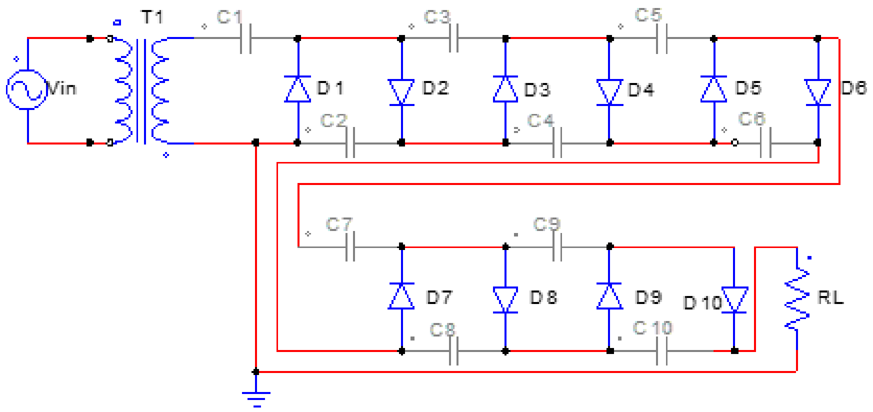

Figure 1. Schematic diagram of Cockcroft–Walton (CW).

The design of the CW multiplier circuit is based on achieving a target high-voltage output while minimizing ripple and losses. The key parameters considered in this design include the number of stages, capacitor values, diode specifications, and operating frequency. The number of stages (nnn) is selected based on the desired output voltage. In this study, the multiplier is designed with **5 stages** to achieve a high-voltage output in the kilovolt range. Capacitors play a crucial role in determining the ripple and voltage stability. The following considerations are applied: Capacitance value 10 nF, and low equivalent series resistance (ESR) to reduce losses.

In addition, diodes must withstand high reverse voltages and fast switching conditions with the following specifications: High-voltage diodes (e.g., ≥ 10 kV rating), fast recovery characteristics, and low forward voltage drop to improve efficiency. The main design specifications of the proposed system are summarized shown in Table 1.

Table 1. Design specifications Cockcroft–Walton.

Parameter	Value
Input Voltage	20 V AC
Frequency	1 kHz
Number of Stages	5 stages
Capacitor Value	10 nF
Transformator step--up	1:10
Load Type	Resistive

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3. RESULT AND DISCCUSSION

Simulation and measurement results of a high-voltage generation system based on a Cockcroft–Walton (CW) multiplier show distinctive characteristics: a gradual increase in voltage with the number of stages, but with an output waveform that does not completely follow the input waveform. The input signal (Vin) has a sinusoidal waveform with a relatively small amplitude compared to the output voltage at each stage. Meanwhile, the voltage at each stage (Stage 1 to Stage 5) shows a significant increase in DC level, but with relatively small fluctuations or ripple compared to the average voltage, as shown in Figure 2-5.

Figure 2-3 shows that Stage 1 produces a voltage of approximately 1 kV, then gradually increases to approximately 9 kV at Stage 5. Theoretically, this phenomenon aligns with the operating principle of a CW multiplier, where the output voltage is the result of the accumulated voltage of each capacitor, gradually charged through a charge-pump process during the positive and negative cycles of the input signal. However, if we look more closely, there is an interesting anomaly, namely the output waveform tends to be “flat” (DC-like) even though the input is a sinusoidal AC signal.

This phenomenon can be explained by the working mechanism of a CW multiplier, which does not transfer the waveform directly, but rather transforms energy through the charging and discharging of capacitors. During the positive half-cycle, the capacitor at a certain stage is charged through a forward-biased diode, while during the negative half-cycle, the energy is transferred to the next stage. As a result, the output voltage is not a replica of the input signal, but rather the result of integrating the energy stored in the capacitors. This causes the output waveform to tend towards DC voltage with small ripples, rather than a sinusoidal waveform like the input.

Intuitively, a voltage increase several times the input might be considered an anomaly, but in the context of a CW multiplier, it is a key characteristic of the system. The high voltage is generated through the voltage stacking effect of each capacitor. However, this increase is not completely linear, as predicted by the ideal model. The graph shows that the voltage increase between stages is not perfectly identical, indicating system losses.

In Figure 3, which displays Stages 3 and 4, the voltage has reached an intermediate level (around 5–7 kV), but the waveform still exhibits DC characteristics with small ripples. This confirms that after some initial stages, the system begins to reach a steady-state condition where the output voltage is stable despite small fluctuations due to the capacitor charging dynamics.

Meanwhile, at Stage 5, the voltage reaches its maximum value in the system, but the voltage increase is not as large as theoretically expected. This indicates performance saturation, where additional stages no longer provide a significant voltage increase. This phenomenon is common in CW multipliers and is caused by accumulated losses and limited energy transfer between stages. This CW circuit does not maintain the input waveform, but instead converts it to a high DC voltage through a charge-pump mechanism. The large amplitude difference and the waveform change from sinusoidal to quasi-DC are evidence that the energy conversion process is working well.

Furthermore, this system design has succeeded in producing high voltage with relatively low ripple, although there are still deviations from ideal conditions. Therefore, further optimization can be carried out by increasing the operating frequency, using higher-quality components, and optimizing the number of stages to achieve a balance between output voltage and system efficiency.

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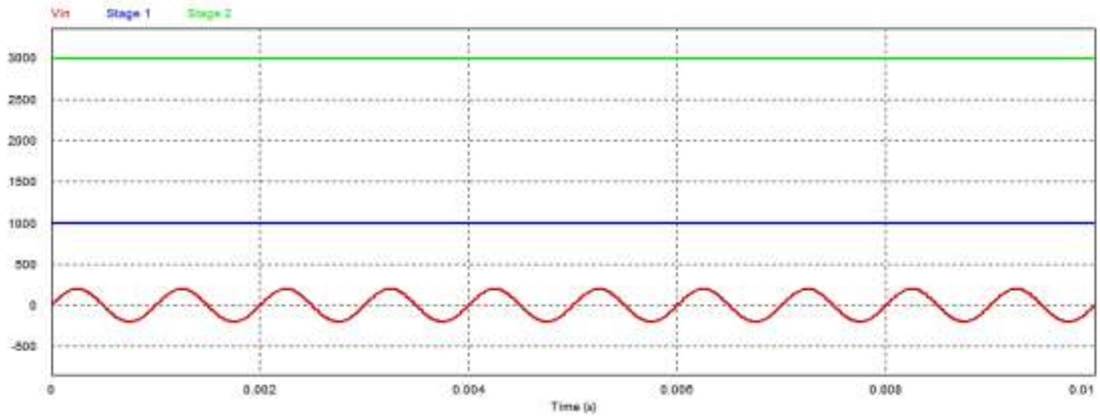

Figure 2. Output voltage of stages 1, 2.

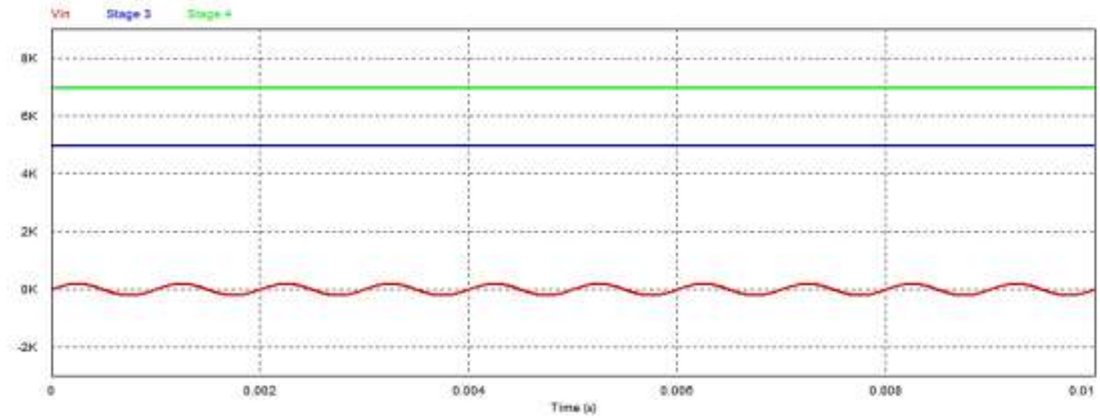

Figure 3. Output voltage of stages 3, 4.

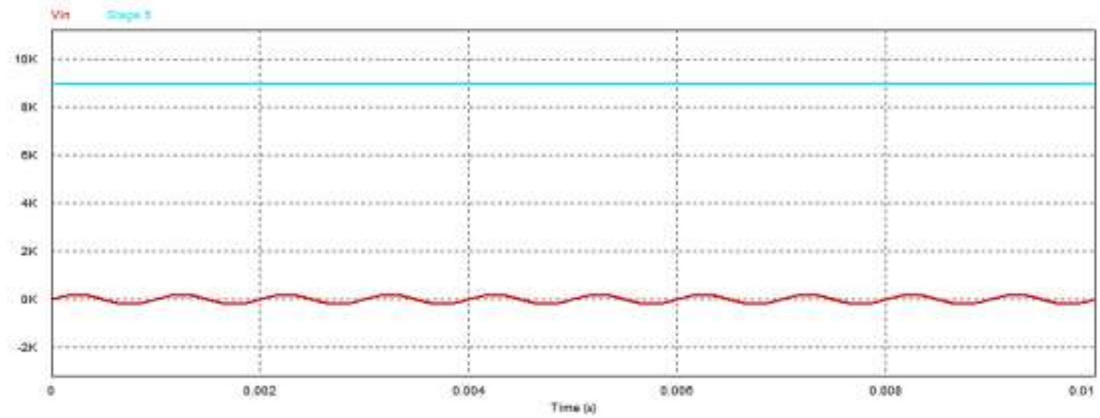

Figure 4. Output voltage of stage 5.

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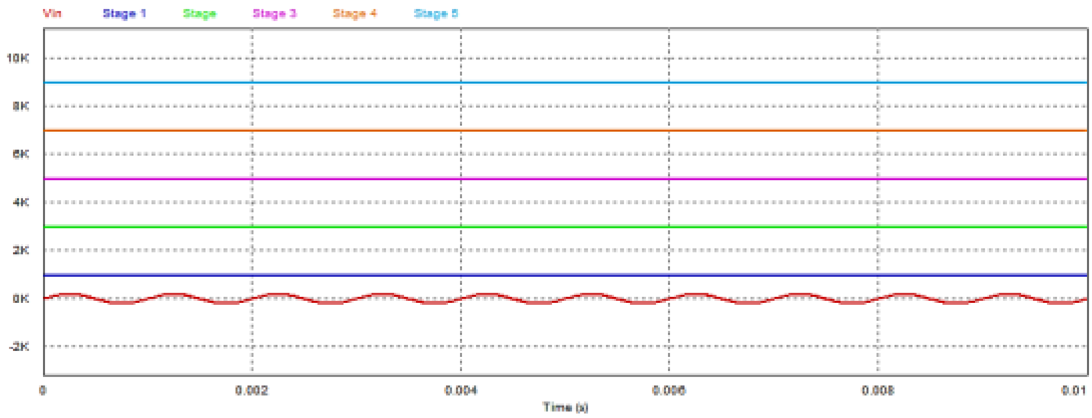

Figure 5. Comparison of output voltage stage 1-5.

The comparison between theoretical and experimental results indicates that the system achieves approximately 86% of the ideal output voltage, demonstrating good agreement with analytical predictions. The efficiency of this CW circuit reaches70.8%. This confirms that the proposed design effectively translates theoretical principles into practical implementation.

4. CONCLUSION

This study presents the proposed system successfully demonstrates the capability to generate high DC voltage in the range of several kilovolts using a compact and modular configuration. The experimental results show strong agreement with theoretical predictions, with the system achieving up to 86% of the ideal output voltage under no-load conditions. The implemented design achieves a satisfactory efficiency of 70.8%, which is considered adequate for educational and low-power applications. Furthermore, ripple voltage is maintained within an acceptable range, making the system suitable for laboratory experiments that do not require highly regulated DC output. The compact design, combined with relatively low cost and ease of implementation, makes the proposed system a viable alternative to conventional high-voltage generation methods that rely on bulky and expensive transformers.

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